Product Specification Sheet

Customer :

Model Name : HAM0667-T

Date : **2023-09-15**

Version : **Ver 1.0**

Customer’s Approval		---	
Signature	Date	Approved By	Date
		Reviewed By	Date
		Prepared By:	Date

Record of Revision

Version	Revise Date	Page	Content
V1.0	2023/09/15		
V2.0			

Contents

1 General Description

1.1 Features

1.1.1 6.67” Flexible AMOLED Panel

1.1.2 Supported 20 : 9 FHD(2400×1080 pixels) Resolution

1.1.3 Green Design

1.1.4 Driving Frequency: support 60Hz & 120Hz;

1.2 Specifications Summary

No.	Item	Unit	Specification	Note
1	Screen size	inch	6.67	
2	Resolution	dot	2400×1080 (SPR)	
3	Display mode	--	AMOLED	
4	Aspect Ratio	--	20 : 9	
5	Active area	mm	154.56mm*69.552mm	
6	Outline Dimension	mm	165.16mm*71.532mm (before bending)	MOD W/O CG
7	Driver IC	--	VTDR6130	
8	Touch IC	--	FT3658U	
9	IC Location	--	Driver IC : COP Touch IC : FPC	
10	Touch Sensor	--	DOT	
11	Interface	--	Drive : MIPI Touch : IIC	

2 Electrical Specifications

2.1 Main FPC Pin Assignment—AMOLED Panel Input / Output Signal Interface

Connector Type：BF035-I40B-C08-D

Pin No.	Symbol	I/O	Description	Notes
1	GND	P	Ground.	
2	ELVSS	P	Power Supply Input for Panel(-)	
3	D3N	I	DSI-D3+/- differential data signals of MIPI	
4	ELVSS	P	Power Supply Input for Panel(-)	
5	D3P	I	DSI-D3+/- differential data signals of MIPI	
6	VOTP(DUMMY)	-	- Not connected.	
7	GND	P	Ground.	
8	ELVDD	P	Power Supply Input for Panel(+)	
9	D0N	I	DSI-D0+/- differential data signals of MIPI	
10	ELVDD	P	Power Supply Input for Panel(+)	
11	D0P	I	DSI-D0+/- differential data signals of MIPI	
12	VCI	P	Power Supply Input for Analog Circuit	
13	GND	P	Ground.	
14	AVDD	P	Power Supply Input for Analog Circuit	
15	CKN	I	DSI-CLK+/- differential data signals of MIPI	
16	IOVCC	P	Power Supply Input for Digital Circuit	
17	CKP	I	DSI-CLK+/- differential data signals of MIPI	
18	OLED_EN	O	AVDD_EN signal for PMIC	
19	GND	P	Ground.	
20	EL_CTRL	O	Swire signal for PMIC	
21	D1N	I	DSI-D1+/- differential data signals of MIPI	
22	TE	O	DIC TE signal	
23	D1P	I	DSI-D1+/- differential data signals of MIPI	
24	DUMMY	-	- Not connected.	
25	GND	P	Ground.	
26	GND	P	Ground.	
27	D2N	I	DSI-S2+/- differential data signals of MIPI	
28	DUMMY	-	- Not connected.	
29	D2P	I	DSI-S2+/- differential data signals of MIPI	
30	DUMMY	-	- Not connected.	
31	GND	P	Ground.	
32	DUMMY	-	- Not connected.	
33	RESET	I	RESET FOR DIC	

Pin No.	Symbol	I/O	Description	Notes
34	DUMMY	-	- Not connected.	
35	DUMMY	-	- Not connected.	
36	GND	P	Ground.	
37	TP_INT	O	TIC IIC interface interrupt signal	
38	TP_SDA	I	TIC IIC interface data	
39	TP_SCL	I	TIC IIC interface clock	
40	TP_VDD	P	Analog power supply input for TIC	

Note : I (Input); O (Output); P (Power); I/O (Input /Output);

2.2 Absolute Maximum Ratings

2.2.1 Module Panel Absolute Maximum Ratings

Item	Symbol	Value		Unit	Remark
		Min.	Max.		
Digital Power Supply	VDDIO	-0.3	2.0	V	Note1
Analog Power Supply	VCI	-0.3	5.5	V	
Digital Power Supply	DVDD	-0.3	1.26	V	
Power Supply For Analog Circuit.	AVDD	-0.3	8.8	V	
ELVDD Power Supply	ELVDD	-0.3	6	V	Note2
ELVSS Power Supply	ELVSS	-5	0.3	V	
Operating Temperature(Ambient)	Top	-	-	℃	Refer to RA test result
Storage Temperature(Ambient)	Tstg	-	-	℃	
Humidity	Hstg	-	-	%RH	

Note1: If the module exceeds the absolute maximum ratings, it may be damaged permanently.

Note2:

3 Electrical Characteristics

3.1 Display DC Characteristics &Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
ELVDD	ELVDD	-	-	4.6	-	V	Controlled By DDIC
ELVSS	ELVSS	-	-	Normal : -3.4 HBM : -4.3 AOD : -2.0	-	V	
AVDD	AVDD	-	-	7.6	-	V	
DVDD	DVDD		1.1	1.2	1.23	V	
VCI	VCI	-	2.65	3.0	4.8	V	-
VDDIO	VDDIO	-	1.65	1.8	1.95	V	-
Current Consumption	AVDD	Frame f=120Hz Normal/500nits White pattern	-	26.494	-	mA	Note1
	DVDD			51.168		mA	
	VCI		-	10.878	-	mA	
	VDDIO		-	3.424	-	mA	
	ELVDD		-	330.143	-	mA	
	ELVSS		-	329.884	-	mA	
	AVDD	Frame f=120Hz HBM/700nits White pattern	-	25.784	-	mA	
	DVDD			52.564		mA	
	VCI		-	10.884	-	mA	
	VDDIO		-	3.432	-	mA	
	ELVDD		-	233.38	-	mA	
	ELVSS		-	233.058	-	mA	

Note1: Average of 5pcs Module Panel

3.2 Touch DC Characteristics &Current Consumption

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
AVDD	TP_VDD	-	2.7	3.0	3.3	V	
VDDIO	TP_VDDIO	-	1.65	1.8	3.3	V	
Power Consumption	Active With one finger		-	88.73	-	mW	Note1
	Idle Mode		-	6.72	-	mW	
	Sleep Mode		-	0.3	-	mW	
	Gesture Mode		-	-	-	mW	

Note1: Average of 5pcs Module Panel

3.3 SPI Interface Characteristic

3.3.1 Data to Clock Timing Definitions

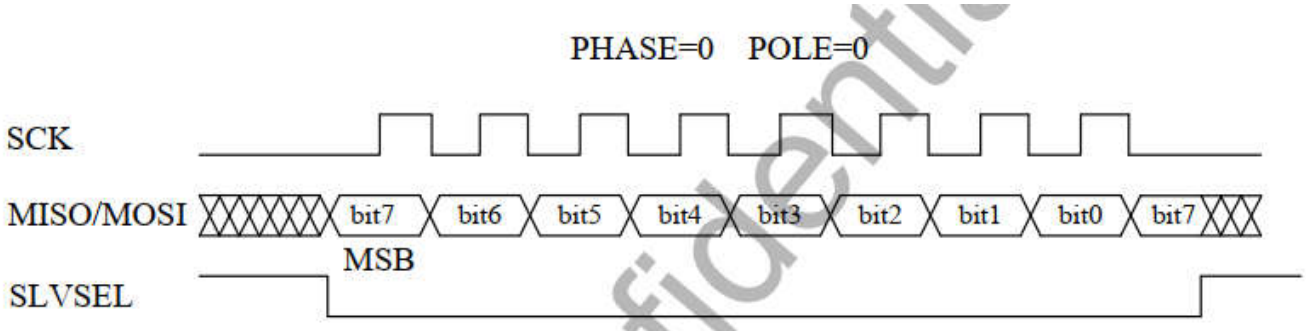


Figure 2-9 SPI Data Transfer Format (Phase=0, POLCK=0)

Table 2-3 SPI Timing Parameters

Parameter	Description	Min	Max	Units
Master Mode timing (see figure 2-11,2-12)				
Tmckh	sck high time	4×Tsysclk	--	ns
Tmckl	sck low time	4×Tsysclk	--	ns
Tmo	sck shift edge to mosi data change	0	--	ns
Tmh	mosi data valid to sck shift edge	3×Tsysclk	--	ns
Tsd	slvsel falling edge to mosi data valid	4×Tsysclk	--	ns
Tmsfc	slvsel falling edge to first sck edge	(Tmckh+Tmckl)/2	--	ns
Tmsrc	last sck edge to slvsel rising edge	(Tmckh+Tmckl)/2	--	ns
Slave mode timing(See figure 2-13,2-14)				
Tsckh	sck high Time	4×Tsysclk	--	ns
Tsckl	sck low Time	4×Tsysclk	--	ns
Tsd	slvsel falling edge to Miso valid data time	0	4xTsysclk	ns
Ts	Mosi Data valid to sck sample edge	0	--	ns
Th	sck sample edge to Mosi data change	4×Tsysclk	--	ns
To	sck shift edge to Miso data change	0	4xTsysclk	ns
Tsfc	slvsel falling edge to first sck edge	4×Tsysclk	--	ns
Tsrc	last sck edge to slvsel rising edge	4×Tsysclk	--	ns
*Tsysclk is equal to one period of the device system clock				

3.4 MIPI Interface Characteristic

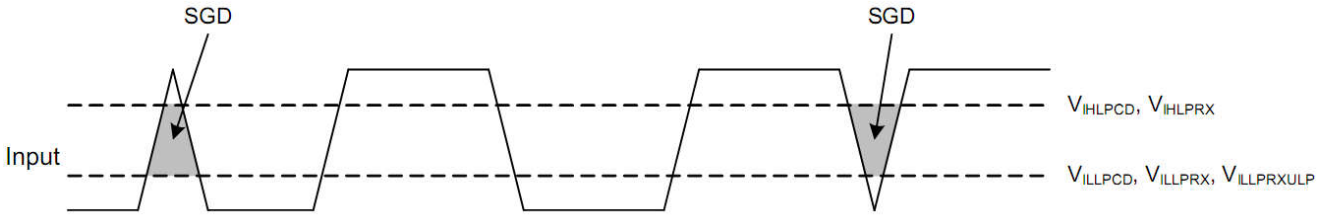
3.4.1 DC Characteristics for D-PHY LP Mode

Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Logic high level input voltage	V_{IHLPCD}	LP-CD	450	-	1350	mV
Logic low level input voltage	V_{ILLPCD}	LP-CD	0	-	200	mV
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK, D0, D1)	880	-	1350	mV
Logic low level input voltage	V_{ILLPRX}	LP-RX (CLK, D0, D1)	0	-	550	mV
Logic low level input voltage	$V_{ILLPRXULP}$	LP-RX (CLK ULP mode)	0	-	300	mV
Logic high level input voltage	V_{OHLPTX}	LP-TX (D0)	1.1	-	1.3	V
Logic low level input voltage	V_{OLLPTX}	LP-TX (D0)	-50	-	50	mV
Logic high level input voltage	I_{IH}	LP-CD, LP-RX	-	-	10	μA
Logic low level input voltage	I_{IL}	LP-CD, LP-RX	-10	-	-	μ
Input pulse rejection	SGD	DSI2-CLK+/-, DSI2-Dn+/-	-	-	300	Vps

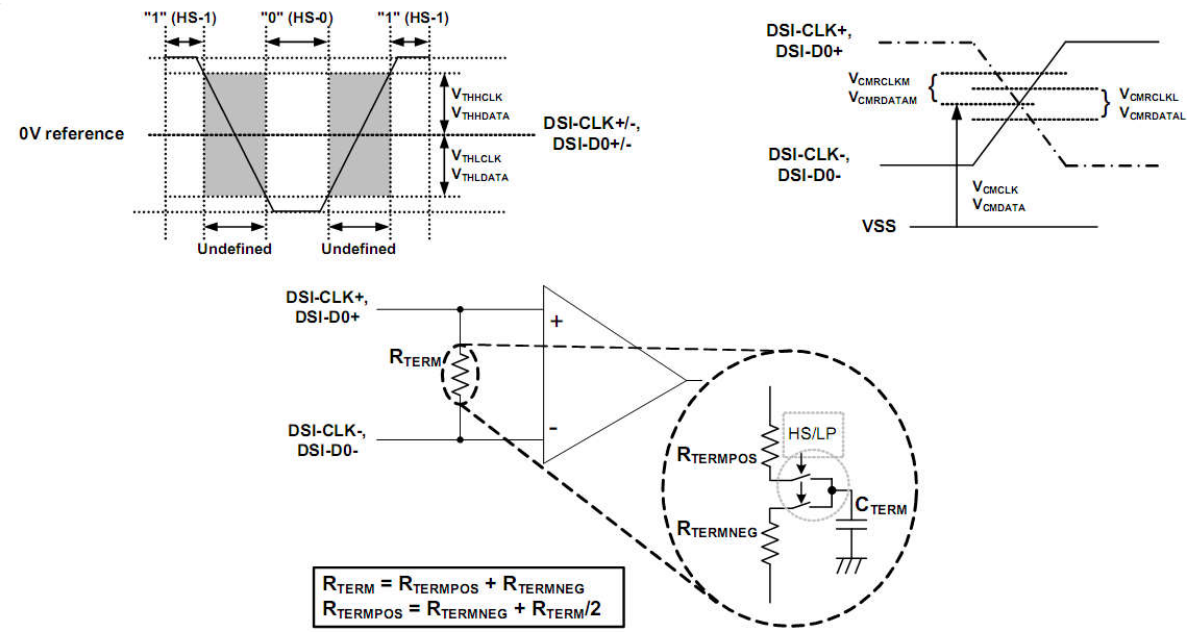
Note 1) VDDI=1.65~1.95V, DVSS=AVSS=VSSR=VSSB=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).

Note 2) DSI2 high speed is off.

Note 3) Peak interference amplitude max. 200mV and interference frequency min. 450MHz.



3.4.2 DC Characteristics for D-PHY HS Mode



Parameter	Symbol	Conditions	Specification			Unit
			Min.	Typ.	Max.	
Input Voltage Common Mode Range	V_{CMCLK} V_{CMDATA}	DSI2-CLK+/-, DSI2-Dn+/- (Note2, 3)	70	-	330	mV
Input Voltage Common Mode Variation (≤ 450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	DSI2-CLK+/-, DSI2-Dn+/- (Note4)	-50	-	50	mV
Input Voltage Common Mode Variation (≥ 450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	100	mV
Low-level Differential Input Voltage Threshold	V_{THLCLK} $V_{THLDATA}$	DSI2-CLK+/-, DSI2-Dn+/-	-70	-	-	mV
High-level Differential Input Voltage Threshold	V_{THHCLK} $V_{THHDATA}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	70	mV
Single-ended Input Low Voltage	V_{ILHS}	DSI2-CLK+/-, DSI2-Dn+/-	-40		-	mV
Single-ended Input High Voltage	V_{IHHS}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	460	mV
Differential Input Termination Resistor	R_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	80	100	125	Ω
Single-ended Threshold Voltage for Termination Enable	$V_{TERM-EN}$	DSI2-CLK+/-, DSI2-Dn+/-	-	-	450	mV
Termination Capacitor	C_{TERM}	DSI2-CLK+/-, DSI2-Dn+/-	-	-	14	pF

Note 1) VDDI=1.65~1.95V, DVSS=AVSS=VSSR=VSSB=VSSAM=0V, Ta=-30 to 70 ºC (to +85 ºC no damage).

Note 2) Includes 50mV (-50mV to 50mV) ground difference.

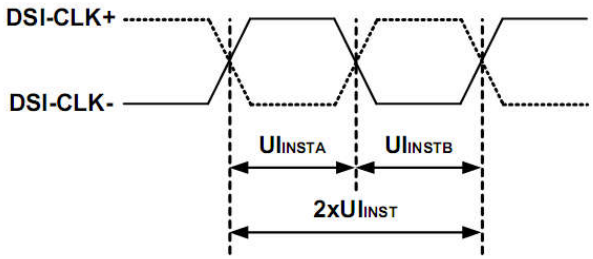
Note 3) Without VCMRCLKM / VCMRDATAM .

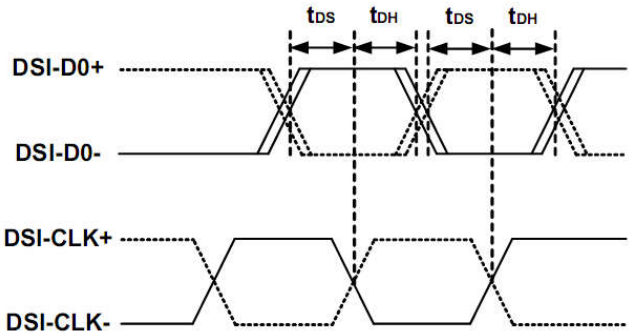
Note 4) Without 50mV (-50mV to 50mV) ground difference.

Note 5) Dn=D0, D1, D2 and D3.

3.4.3 MIPI DSI2 Timing Characteristics

3.4.3.1 D-PHY High Speed Mode





Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
DSI2-CLK+/-	$2xUI_{INST}$	Double UI Instantaneous	1.67	-	4	ns	4 Lane (Note 2)
DSI2-CLK+/-	UI_{INSTA} UI_{INSTB}	UI Instantaneous Halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	0.83	-	2	ns	4 Lane (Note 2)
DSI2-Dn+/-	tDS	Data to Clock Setup Time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI		-		Note 1, 4
DSI2-Dn+/-	tDH	Data to Clock Hold Time	0.15xUI	-	-	ps	Note 1, 3
			0.2xUI		-		Note 1, 4
DSI2-CLK+/- DSI2-Dn+/-	tDRTCLK	Differential Rise Time for Clock	-	-	0.3xUI	ps	Note 1, 5
			-	-	0.35xUI		Note 1, 6
			100	-	-		Note 1, 7

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is TBD Gbps for 24-bit data format which support to 1440RGBx3360 resolution.

Note 3) Total setup and hole window for receiver of 0.3 UIINST when D-PHY is supporting maximum data rate = 1Gbps.*

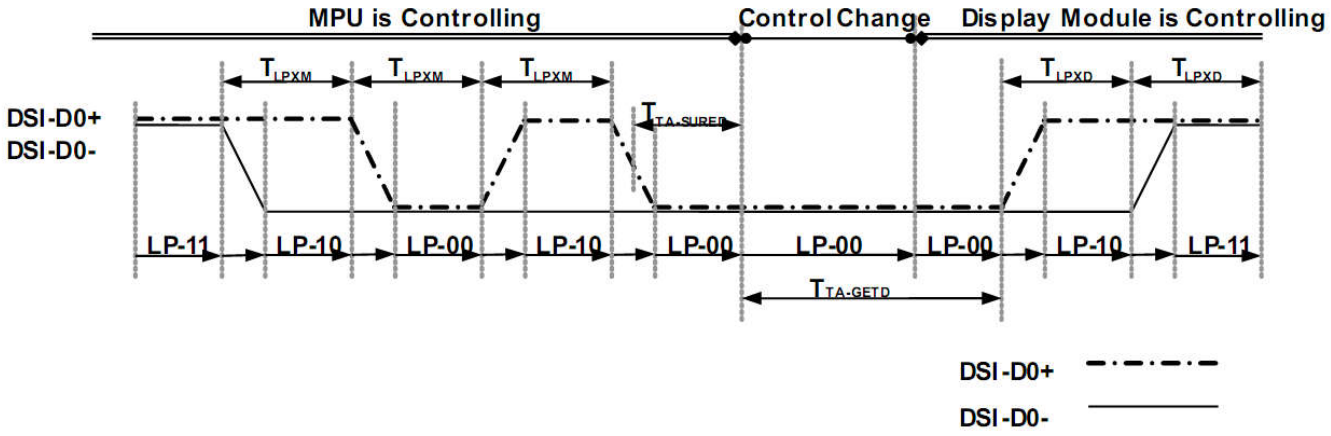
Note 4) Total setup and hole window for receiver of 0.4 UIINST when D-PHY is supporting maximum data rate > 1Gbps.*

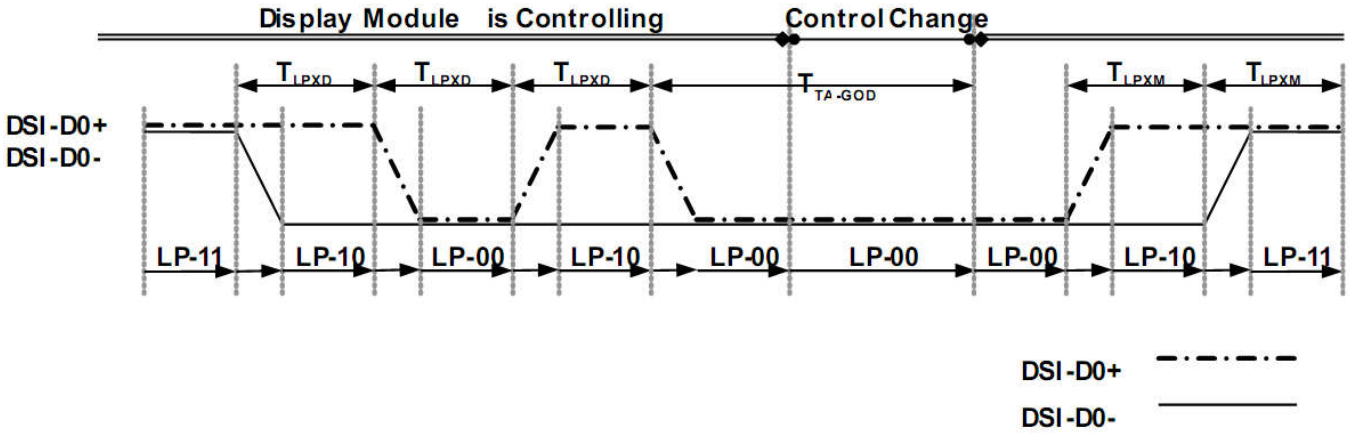
Note 5) Applicable when operating at HS bit rates ≤ 1 Gb ps (UI ≥ 1 ns).

Note 6) Applicable when operating at HS bit rates > 1 Gbps (UI < 1 ns).

Note 7) Applicable for all HS b it rates. However, to avoid excessive radiation, b it rates ≤ 1 Gb ps (UI ≥ 1 ns), should not use values below 150 ps.

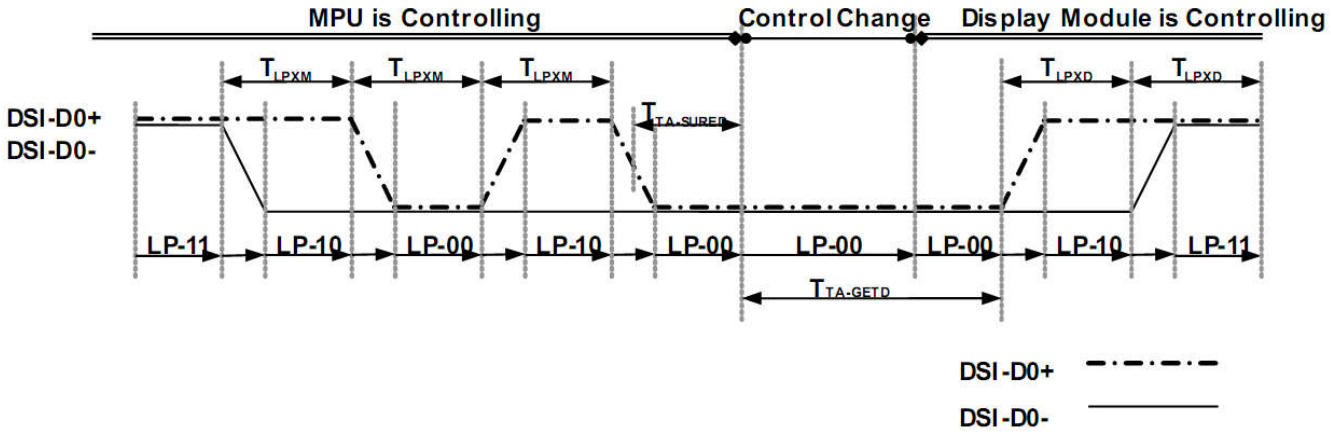
3.4.3.2 D-PHY Low Power Mode

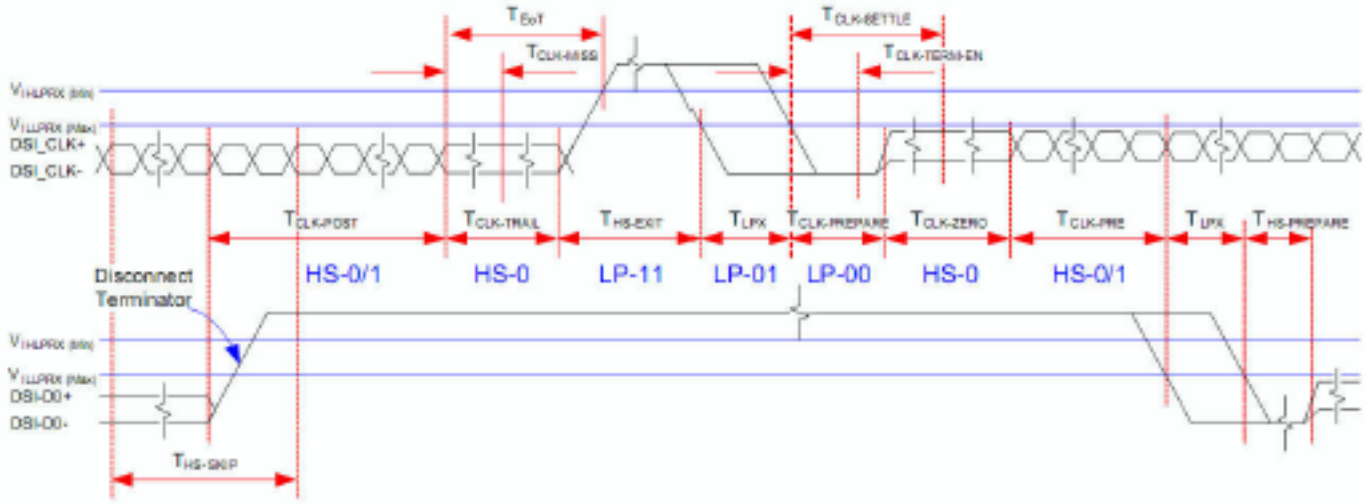




Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
DSI2-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 Periods MPU Display Module	50	-	75	ns	Input
DSI2-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 Periods Display Module MPU	50	-	75	ns	Output
DSI2-D0+/-	$T_{TA-SURED}$	Time-out Before The MPU Start Driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI2-D0+/-	$T_{TA-GETD}$	Time to Drive LP-00 by Display Module	-	$5xT_{LPXD}$	-	ns	Input
DSI2-D0+/-	T_{TA-GOD}	Time to Drive LP-00 after Turnaround Request MPU	-	$4xT_{LPXd}$	-	ns	Output

3.4.3.3 D-PHY DSI2 Bursts



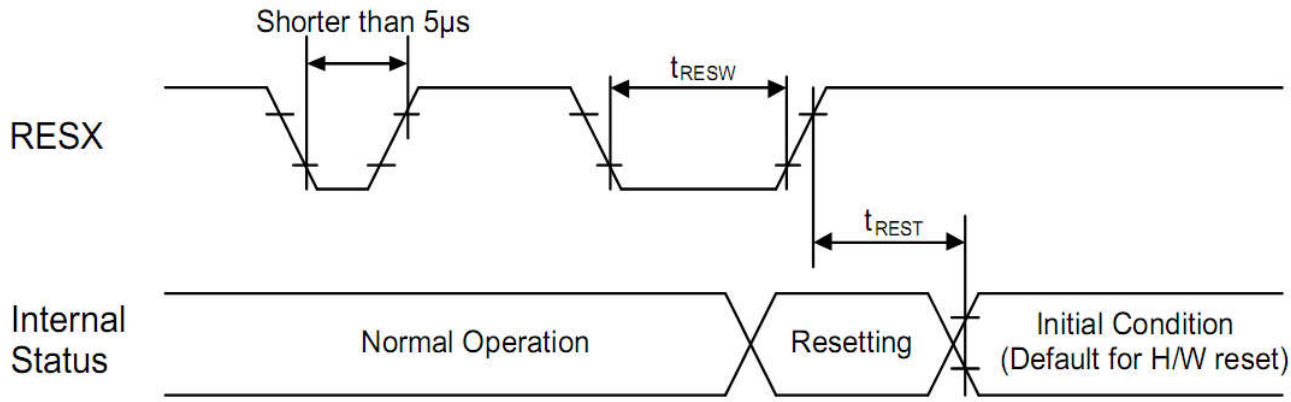


Signal	Symbol	Parameter	Min.	Typ.	Max.	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI2-Dn+/-	T_{LPX}	Length of Any Low Power State Period	50	-	-	ns	Input
DSI2-Dn+/-	$T_{HS-PREPARE}$	Time to Drive LP-00 to Prepare for HS Transmission	40+4xUI	-	85+6xUI	ns	Input
DSI2-Dn+/-	$T_{HS-TERM-EN}$	Time to Enable Data Receiver Line Termination Measured from when Dn Crosses VILMAX	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI2-Dn+/-	$T_{HS-SKIP}$	Time-out at Display Module to Ignore Transition Period of EoT	40	-	55+4xUI	ns	Input
DSI2-Dn+/-	$T_{HS-EXIT}$	Time to Drive LP-11 after HS burst	100	-	-	ns	Input
DSI2-Dn+/-	$T_{HS-TRAIL}$	Time to Drive Flipped Differential State after Last Payload Data Bit of a HS Transmission Burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI2-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall Continue Sending HS Clock after the Last Associated Data Lane has Transition to LP Mode	60+52xUI	-	-	ns	Input
DSI2-CLK+/-	$T_{CLK-TRAIL}$	Time to Drive HS Differential State after Last Payload Clock Bit of a HS Transmission Burst	60	-	-	ns	Input
DSI2-CLK+/-	$T_{HS-EXIT}$	Time to Drive LP-11 after HS Burst	100	-	-	ns	Input
DSI2-CLK+/-	$T_{CLK-PREPARE}$	Time to Drive LP-00 to Prepare for HS Transmission	38	-	95	ns	Input
DSI2-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at Clock Lane Display Module to Enable HS Transmission	-	-	38	ns	Input
DSI2-CLK+/-	$T_{CLK-PREPARE+}$ $T_{CLK-ZERO}$	Minimum Lead HS-0 Drive Period Before Starting Clock	300	-	-	ns	Input
DSI2-CLK+/-	$T_{CLK-PRE}$	Time that the HS Clock Shall be Driven Prior to Any Associated Data Lane Beginning the Transition from LP to HS Mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as $T_{HS-EXIT}$ from each other in continuous clock mode. In discontinuous mode, the break is longer which account $T_{CLK-POS}$, $T_{CLK-TRAIL}$ and $T_{HS-EXIT}$, before activity in clock and data lanes again.

3.4.4 Reset Input Timing



Signal	Symbol	Parameter	Min	Typ	Max	Unit	Description
RESX	tRESW	Reset "L" pulse width (Note 1)	10	-	-	µs	
	tREST	Reset complete time (Note 2)	-	-	10	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and (Note 4)

Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 30µs	*Reset*
Between 5µs and 30µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

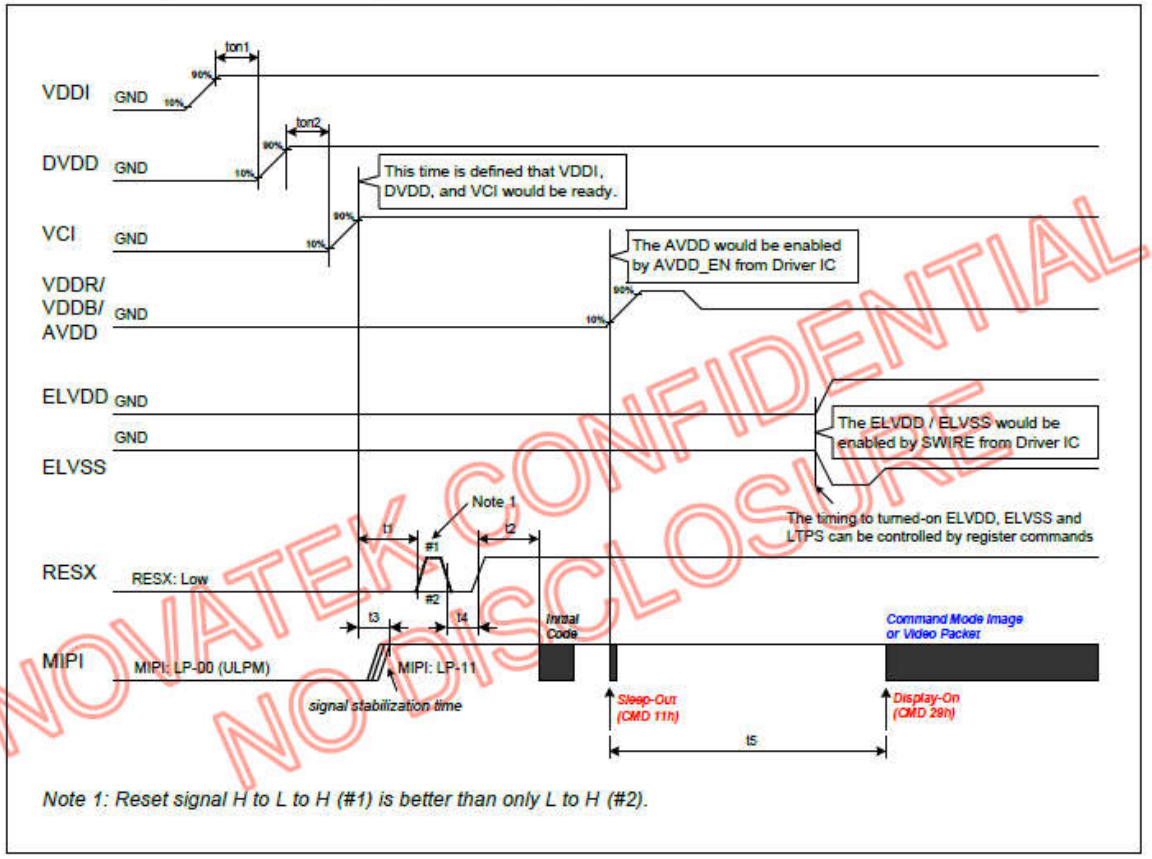
Note 4) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

3.5 Power Sequence

3.5.1 Power On sequence

- 3 Input Power (BTM = "0") with external DVDD (EXT_DVDD_EN = "1")

VDDI=1.65~1.95V, DVDD=1.1~1.23V, VCI=2.65~4.8V, VDDR=VDDB=AVDD=6.0~8.0V



Note1 : Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	-	No Limit	-	ms	
t1	10	-	-	ms	
t2	10	-	-	ms	
t3	0	-	t1	ms	
t4	30	-	-	µs	
t5	120	-	-	ms	

3.5.2 Touch Power On sequence

Reset should be pulled down to be low before powering on and powering down. I2C/SPI shouldn't be used by other devices during Reset time after IOVCC powering on (Tprt). INT signal will be sent to the host after initializing all parameters and then start to report points to the host. If Power is down, the voltage of supply must be below 0.3V and Tpdt is more than 5ms.

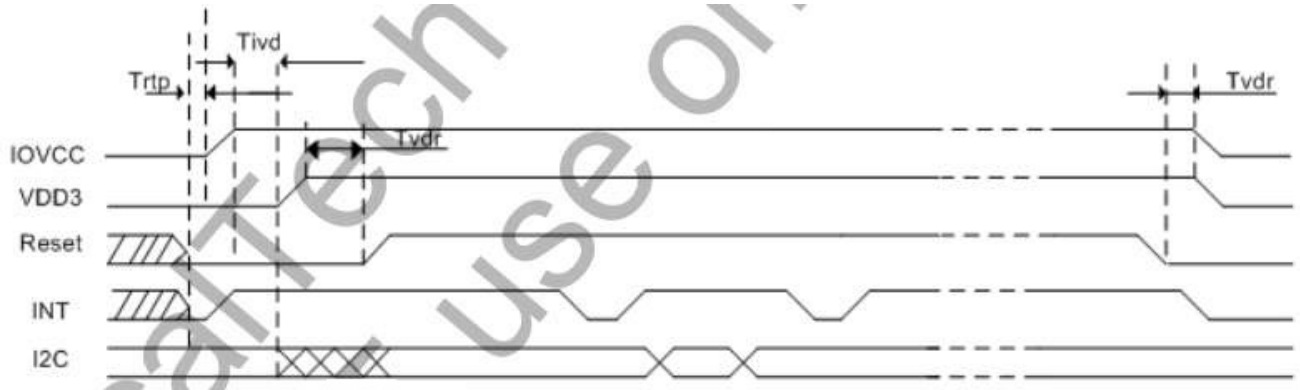


Figure 3-6 Power on-off Sequence

(Note: We recommend that IOVCC be powered on before VDD3(VDDA). At the same time, FT3658U can also support IOVCC to be powered on after VDD3(VDDA) or at the same time for robustness.)

Reset time must be enough to guarantee reliable reset, the time of starting to report point after resetting approach to the time of starting to report point after powering on.

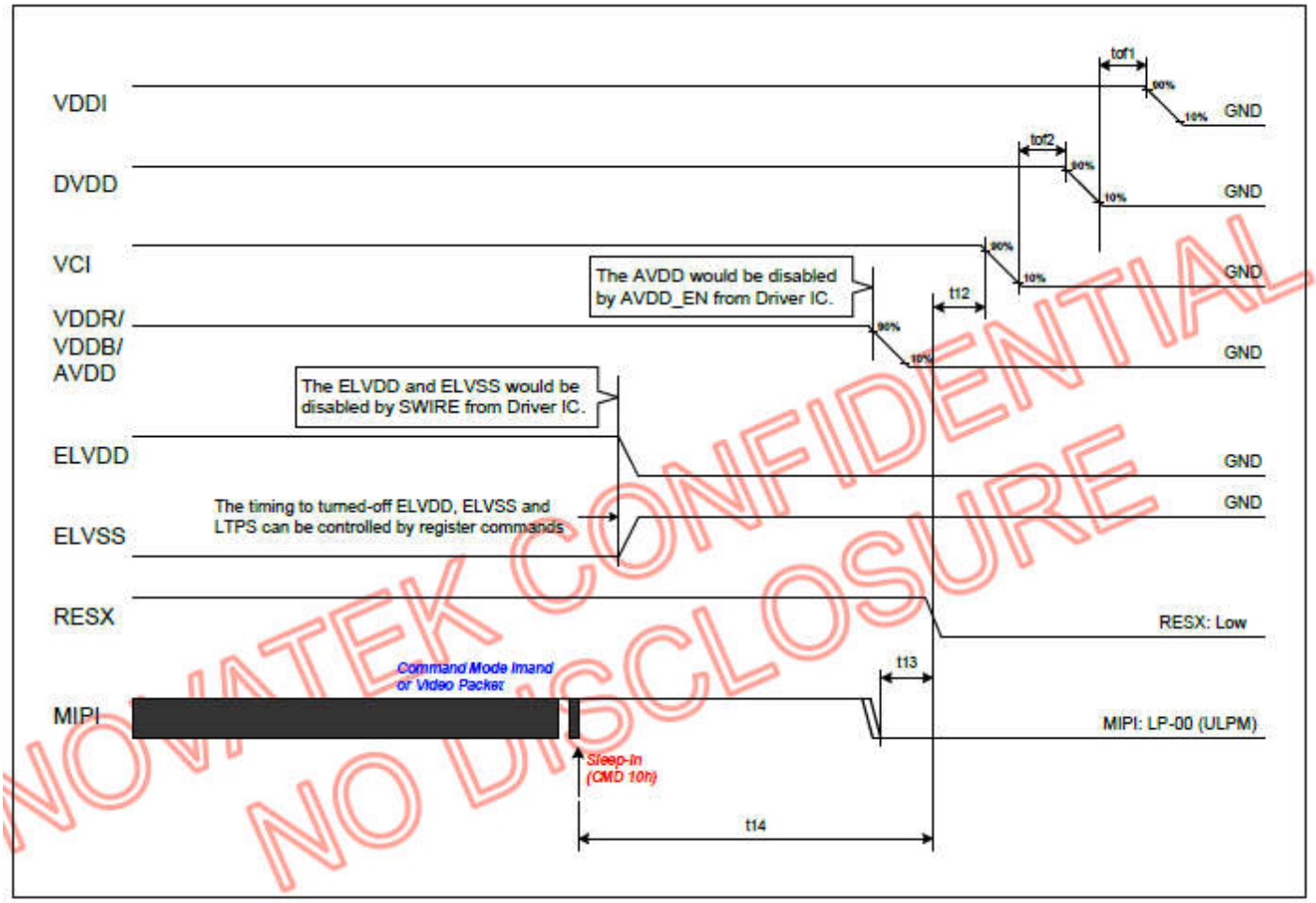
Table 3-5 Power on/Reset/Wake Sequence Parameters

Parameter	Description	Min	Max	Units
Tris	Rise time from 0.1VDD to 0.9VDD	--	5	ms
Tpdt	Time of the voltage of supply being below 0.3V	5	--	ms
Trtp	Time of resetting to be low before powering on	100	--	μs
Tivd	Delay time of VDD powering on after IOVCC	10		μs
Tvdr	Reset time after VDD powering on	1	--	ms
Trsi	Time of starting to report point after resetting	--	200	ms
Trst	Reset time	1	--	ms

3.5.3 Power Off sequence

The power off sequence are shown below figures.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
tof1	0	-	-	ms	
tof2	-	No limit	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	-	100	-	ms	



3.6 Touch Electrical Test Item

3.6.1 Test Item

Test Item	Note
download	烧录
rst pin test	复位测试
fw version	fw 版本号测试
enter factory	进入测试模式
channel num	通道数测试
raw data	容值测试
rawdata uniformity	容值均一性测试
scap cb	自容 Cb 测试
scap rawdata	自容 Rawdata
panel differ	感应量测试
weak short circuit	short 阻抗测试>=1.2M
int pin test	终端测试
sync test	同步信号测试
Ocs calibration	TIC 晶振校正
noise	亮屏噪声测试
Burn Lockdown	Lockdown 烧录
Check Lockdown	Lockdown check

3.6.2 Test Environment

1. Operator must wear the anti-ESD ring before handing.

2. The grounding condition of test fixture is well.

3. The plasma fan must be kept open during the test.

4. Do not touch the screen surface during the test, such as the fingers, the suction nozzle.

3.7 OP manual

3.7.1 Operation Sequence

3.7.1.1 Power On Sequence

Order	Sequence	Remark
1	Power Off Status	
2	System Power On 1. Turn on VCI/VDDI/DVDD	
3	Wait > 10ms	
4	Data, Clk : LP 00→01→11 Activate Reset (System Reset) **1.** RESX = " L " **2.** Wait >30us **3.** RESX = " H " **4.** LP11 > 500us	
5	Wait>10ms	
6	DSC Setting	
7	Common Setting	
8	Sleep Out(11h)	
9	Wait>120ms	
10	Display On(29h)	
11	Display On Status	

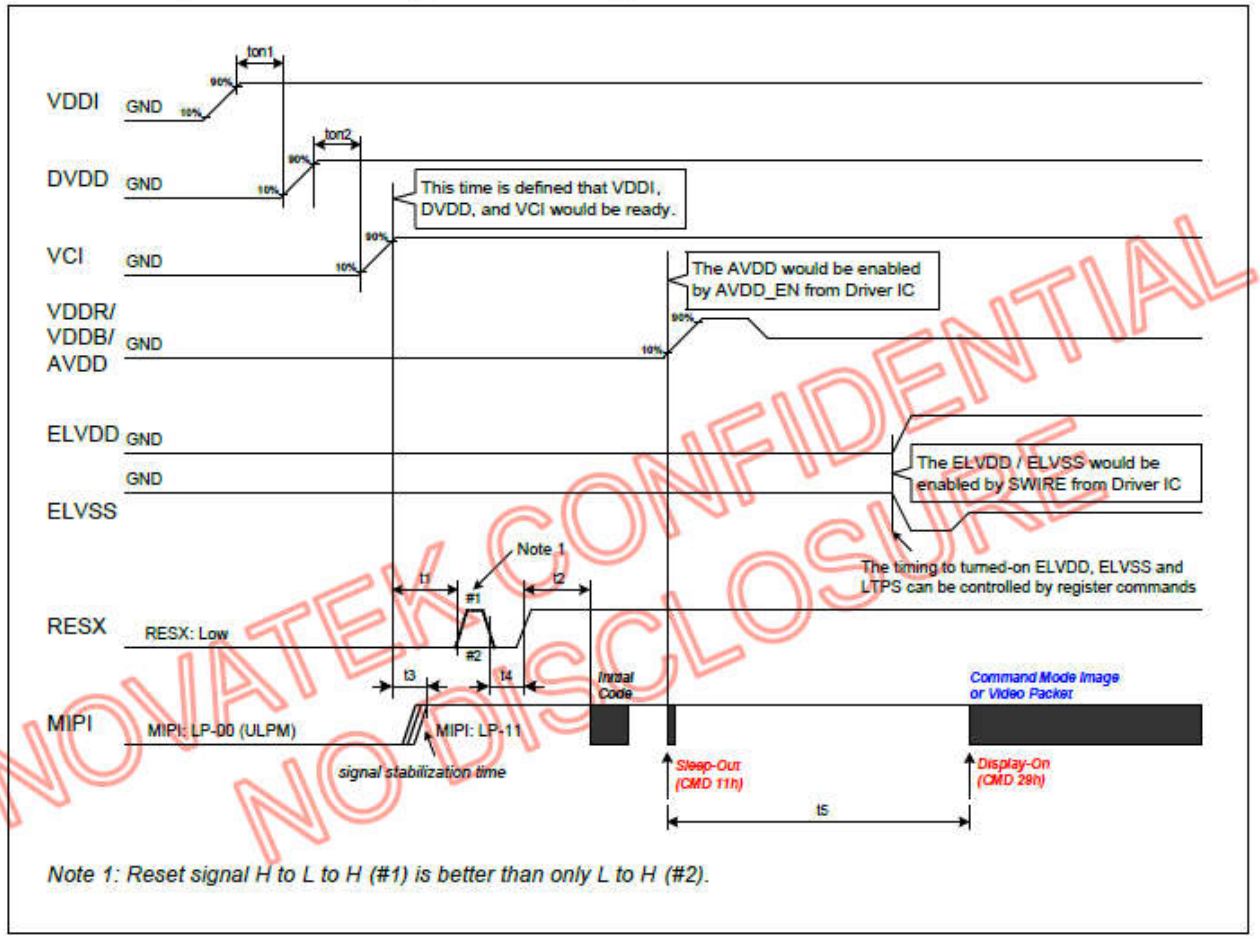
3.7.1.2 Power Off Sequence

Order	Sequence	Remark
1	Display On Status	
2	Display Off (28h)	
3	Wait 10ms	
4	Sleep In (10h)	
5	Wait 120ms	
6	System Power Off 1. Reset " L " 2. Turn off VCI / VDDI/DVDD	
7	Power Off Status	

3.7.1.3 [Note1: System Power on/off]

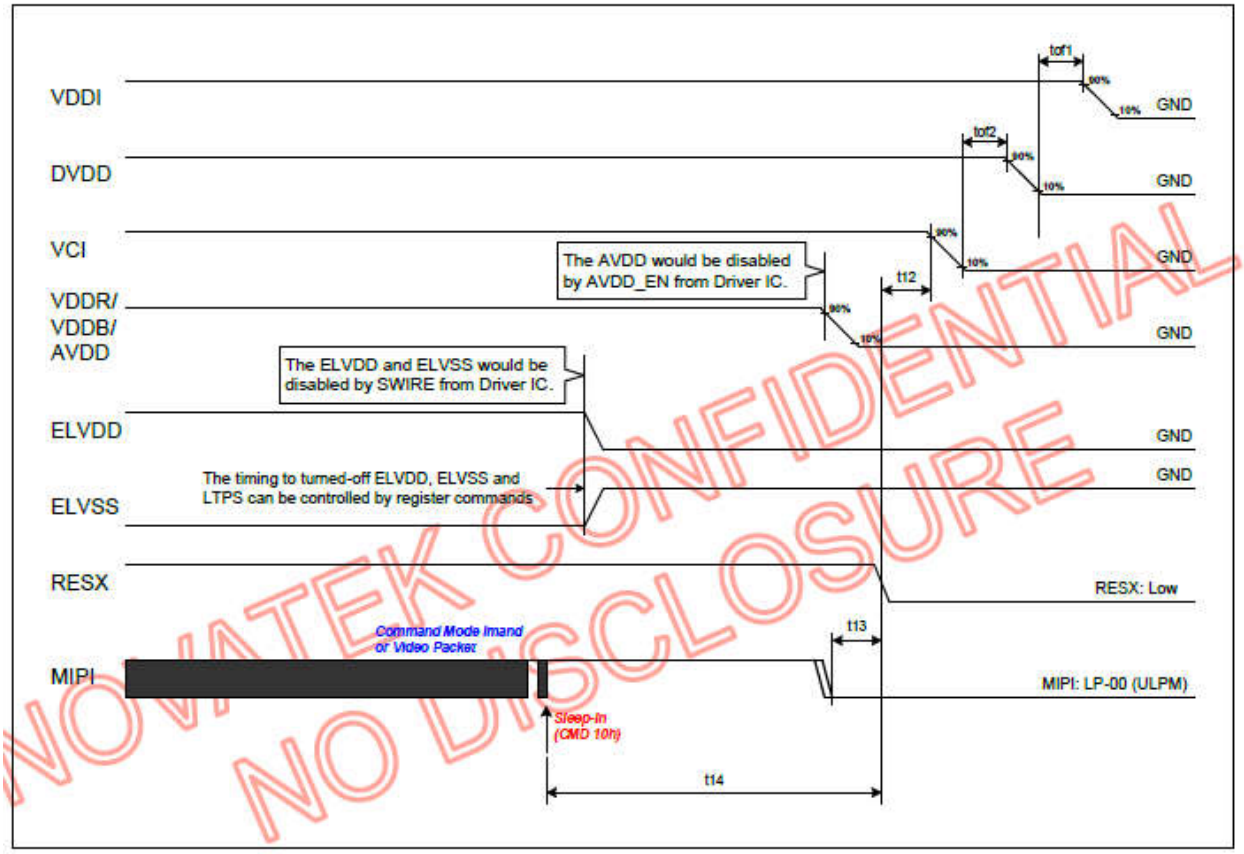
- 3 Input Power (BTM = "0") with external DVDD (EXT_DVDD_EN = "1")

VDDI=1.65~1.95V, DVDD=1.1~1.23V, VCI=2.65~4.8V, VDDR=VDDB=AVDD=6.0~8.0V



Note 1: Reset signal H to L to H (#1) is better than only L to H (#2).

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	0	-	-	ms	
ton2	-	no limit	-	ms	
t1	10	-	-	ms	
t2	10	-	-	ms	
t3	0	-	t1	ms	
t4	30	-	-	µs	
t5	120	-	-	ms	



The power on sequence are shown below figures.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
tof1	0	-	-	ms	
tof2	-	no limit	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	-	100	-	ms	

3.7.1.4 Sleep In Sequence

Order	Sequence	Remark
1	Display On Status	
2	Display Off(28h)	
3	Sleep In (10h)	
4	Wait >120ms	
5	Sleep In Status	

3.7.1.5 Sleep Out Sequence

Order	Sequence	Remark
1	Sleep In Status	
2	Sleep Out (11h)	
3	Wait>120ms	
4	Display On Sequence	

3.7.1.6 Deep Standby In Sequence

Order	Sequence	Remark
1	Display Off (28h)	
2	Sleep In (10h)	
3	Wait >120ms	
4	Enter Deep Standby Mode(4Fh=0x01)	
5	MIPI Drive to LP-00 or Enter ULPM	
6	In Deep Standby Mode	

3.7.1.7 Deep Standby Out Sequence

Order	Sequence	Remark
1	In Deep Standby Status	
2	Set RESX Pin Low > 3ms	
3	Wait >10ms	
4	MIPI Drive to LP-11 or Exit ULPM	
5	DSC Setting	
6	Common Setting	
7	Display On Sequence	

3.7.1.8 AOD on Sequence(Normal → AOD)

Order	Sequence	Remark
1	Normal Display Mode	
2	Enter 60Hz	
3	AOD Mode On	
4	AOD On Status	

3.7.1.9 AOD off Sequence(AOD → Normal)

Order	Sequence	Remark
1	AOD On Status	
2	AOD Mode Off	
3	Normal Display Mode	

3.7.1.10 Enter DC Mode Sequence(Normal → DC Mode)

Order	Sequence	Remark
1	Normal Display On Status	
2	Enter DC Mode Setting	
3	DC Mode	

3.7.1.11 Exit DC Mode Sequence(DC Mode → Normal)

Order	Sequence	Remark
1	DC Mode Status	
2	Exit DC Mode Setting	
3	Normal Display On	

4 Optical Specification

Item	Symbol	Condition	Values			Unit	Notes
			Min.(≥)	Typ.	Max.(≤)		
Color shift	Δu′ v′	Up/Down/Right/Left θ=30°	/	/	3.5	JNCD	Note1 Note2
		Up/Down/Right/Left θ=45°	/	/	5.5		
		Up/Down/Right/Left θ=60°	/	/	6		
Contrast ratio	CR	@0 degree	500,000 : 1	/	/	/	
Viewing angle	CR	@80 degree	1000 : 1	/	/	/	
HBM mode color chromaticity equal to normal mode	RGBWΔx	CIE1931 x	-0.005	0	0.005	/	HBM : 700nit
	RGBWΔy	CIE 1931 y	-0.005	0	0.005	/	
AOD mode color chromaticity equal to normal mode	RGBWΔx	CIE1931 x	-0.008	0	0.008	/	AOD：60nit
	RGBWΔy	CIE 1931 y	-0.008	0	0.008	/	
Color chromaticity (CIE1931)	Wx	CIE1931 x	0.290	0.300	0.310	/	
	Wy	CIE 1931 y	0.305	0.315	0.325		
	Rx	CIE1931 x	0.663	0.683	0.703		
	Ry	CIE 1931 y	0.297	0.317	0.337		
	Gx	CIE1931 x	0.21	0.25	0.29		
	Gy	CIE 1931 y	0.67	0.71	0.75		
	Bx	CIE1931 x	0.104	0.134	0.164		
	By	CIE 1931 y	0.026	0.056	0.086		
Color Gamut	/	DCI P3	98	/	100	%	CIE1931
Luminance (complete machine)	L	/	465	500	535	nits	CPK>1.33
HBM Luminance (complete machine)	L	/	651	700	749	nits	CPK>1.33
AOD Luminance (complete machine)	L	/	/	60/5	/	nits	30Hz
Reflectivity	reflectivity	/	/	/	5	%	以实际一体黑效果为参考(量产POL为住化)
	a	L*a*b	-1.5	0	1.5	/	
	b	L*a*b	-3.0	0	3.0	/	
Response time (first frame on+off)	/	/	/	/	2	ms	
Color uniformity	U%	/	/	/	2	JNCD	W255/W128/ W64
Luminance uniformity	U%	/	80	/	/	%	W255
	U%	/	85	/	/	%	W128/W64
Crosstalk	/	IEC	/	/	2	%	

Item	Symbol	Condition	Values	Unit	Notes	Unit	Notes
			Min.(≥)	Typ.	Max.(≤)		
Lifetime@T95	/	/	300	/	/	Hr	W Pattern
	Δu′ v′	/	/	/	0.004	/	
Gamma	/	L5~L232	2.0	2.2	2.4	/	HBM：700nit
		L233~L240	1.9	2.2	2.5	/	
		L5~L232	2.0	2.2	2.4	/	100nit < L255≤500nit
		L233~L240	1.9	2.2	2.5	/	
		L13~L227	2.0	2.2	2.4	/	10nit < L255≤100nit
		L228~L235	1.9	2.2	2.5	/	
		L25~L222	2.0	2.2	2.4	/	2nit≤L255≤10 nit
		L223~L230	1.9	2.2	2.5	/	
		L13~L227	2.0	2.2	2.4	/	AOD：60nit
		L228~L235	1.9	2.2	2.5	/	
Color shift of white pattern in different DBV register value	Δu′ v′	Condition1	/	/	0.004	/	L255 满足左侧需求
	CCT	Condition2	/	/	400	K	
Image Sticking	/	The Time to < 1 JND(0.004)	/	25	35	s	60HZ
	/	8*8 checker pattern 10s，to G128	/	20	25	min	

Note1：Internal control, to ensure that large Angle of view to the direction of green.

Note2：视角超规部分以主观限样为准；

Test Conditions:

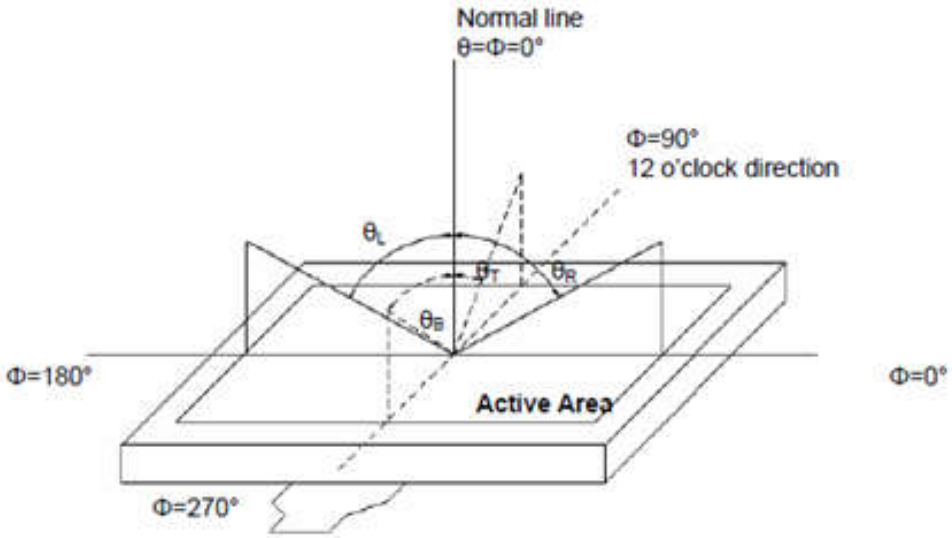
Condition1： max(duv of (DBV level min- max))-min (duv of(DBV level min- max)) , DBV level 1=2nits ;

Condition2： max(CCT of (DBV level min- max))-min(CCT of(DBV level min- max)) , DBV level 1=2nits ;

Condition3： The ambient temperature is 25℃,in dark room

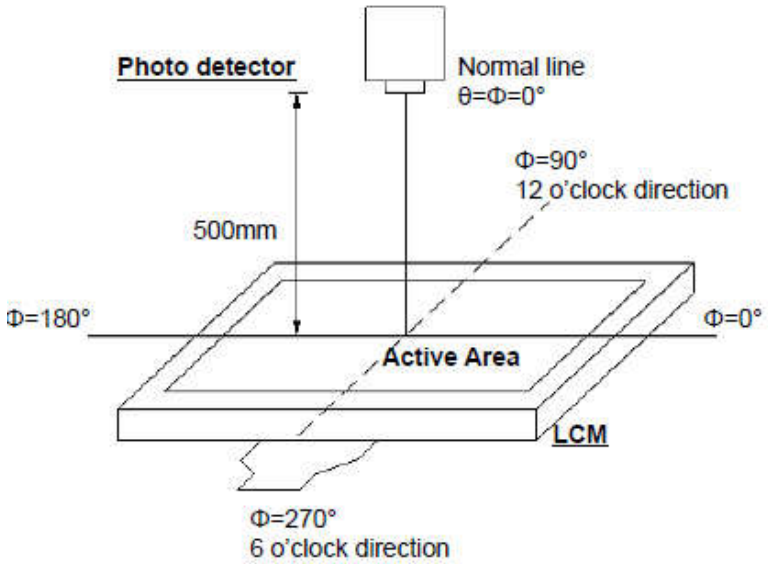
Condition4： The test systems refer to Note 2.

Note 1 : Definition of viewing angle range



Note 2 : Definition of optical measurement system.

The optical characteristics should be measured in dark room. The optical properties are measured at the center point of the OLED screen. (Viewing angle is measured by CS2000A/Height :500mm， Response time is measured by Eldim optiscope200, other items are measured by CS2000A/ spot diameter 8mm /Height: 500mm.)



Note 3 : Definition of contrast ratio

Contrast ratio (CR) = Luminance measured when OLED on the "White" state/ Luminance measured when OLED on the "Black" state

Note 4 : Definition of color chromaticity

White/Red/Green/Blue Color coordinates measured at center point of OLED.

Note 5 : Definition of Luminance

White 255 Gray measured at center point of OLED.

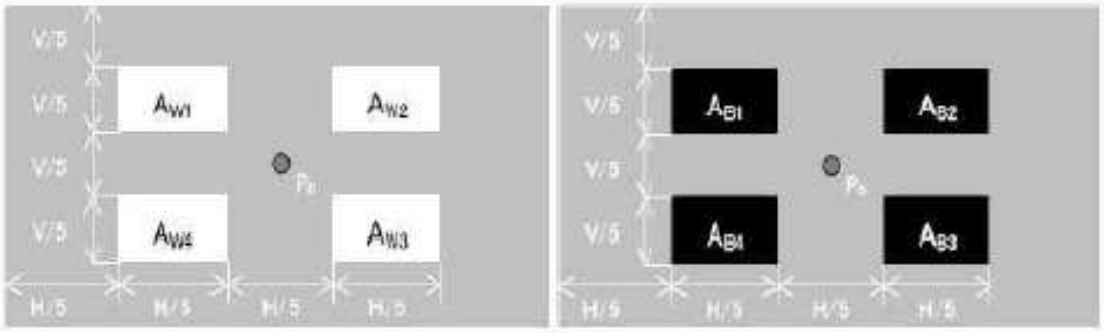
Note 6 : Definition of cross-talk

Measure luminance at the position,P_0

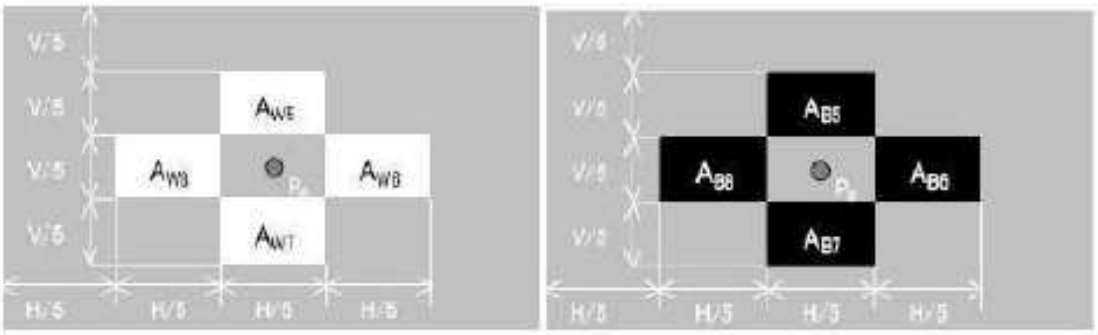
Calculate cross-talk as below equation

$$crosstalk = \frac{|L_{Wi\_ON} - L_{W\_OFF}|}{L_{W\_OFF}} \times 100\% \quad (i = 5\ to\ 8)$$

$$crosstalk = \frac{|L_{Bi\_ON} - L_{B\_OFF}|}{L_{B\_OFF}} \times 100\% \quad (i = 5\ to\ 8)$$



(a) L_{W_OFF}, L_{B_OFF} measuring pattern

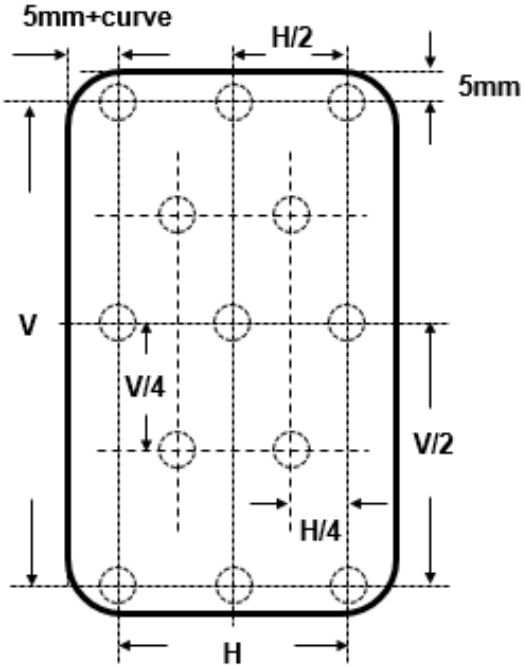


(b) L_{W_ON}, L_{B_ON} measuring pattern

Note 7 : Definition of Luminance Uniformity

Measure the luminance of gray level 255 &128&64 at 13 points

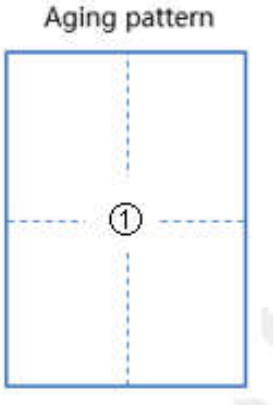
Uniformity = $\frac{Lmin}{Lmax}$ *100%



Note 8 : Definition of Lifetime

Lifetime Measure Steps :

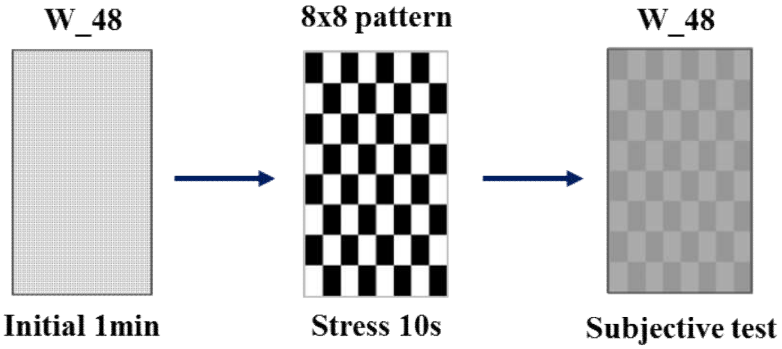
- Light on W Aging pattern for 0.5h befor lifetime measure
- 0h ——W Aging pattern,measure pt.① initial luminance & $\Delta U'V'$
- 0~1h ——W Aging pattern
- 1h ——W Aging pattern,measure pt ① luminance & $\Delta U'V'$
- Loop step below progress ….to 300h



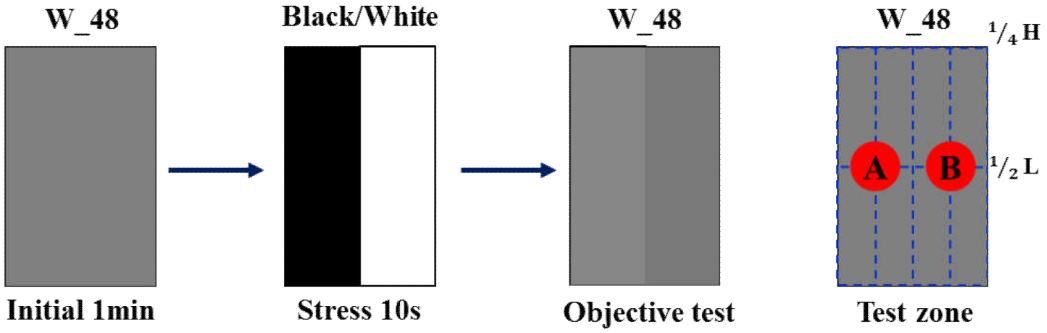
Note 9 : Definition of Image sticking

9.1 Subjective test

1. Test environment temperature is 25℃.
2. Light on W48 pattern for 1min，then change to 8*8 checker pattern for 10s，at last change to W48 pattern and record the time of duration.



9.2 Objective test



Step:

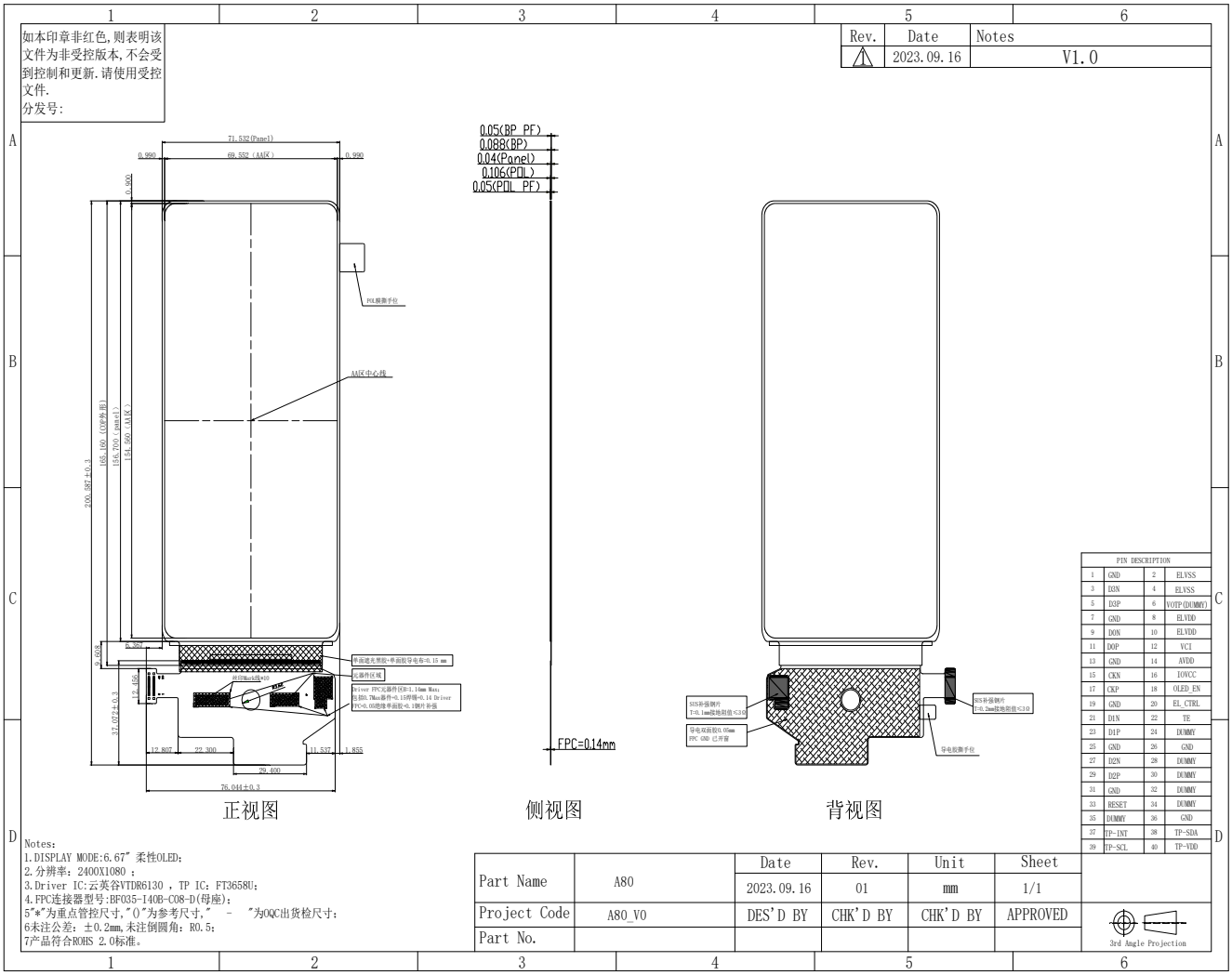
1. Test environment temperature is 25℃.
2. light on 48 gray pattern for 1min，than Change to a black/white pattern for 10s，at last change the pattern back to 48 gray for 1min.
3. Using CA-P410 measures the luminance once a second of test zone in the whole process.
4. Calculate the Michelson contrast value X with formula below：

$$X = \left(\frac{L_{A(t)} - L_{B(t)}}{L_{A(t)} + L_{B(t)}} - \frac{L_{A(Initial\ average)} - L_{B(Initial\ average)}}{L_{A(Initial\ average)} + L_{B(Initial\ average)}}\right)/1JND$$

$$1\ JND = 0.4\%$$

5 Mechanical Characteristics

5.1 Outline Drawing



5.2 Dimension Specifications

Item	Min.	Typ.	Max.	Unit	Note
Width	--	71.532	--	mm	
Height	--	200.587	--	mm	
Depth(w/o PF)	----	----	----	mm	
Weight	--	--	--	mm	

5.3 Module Stack Up

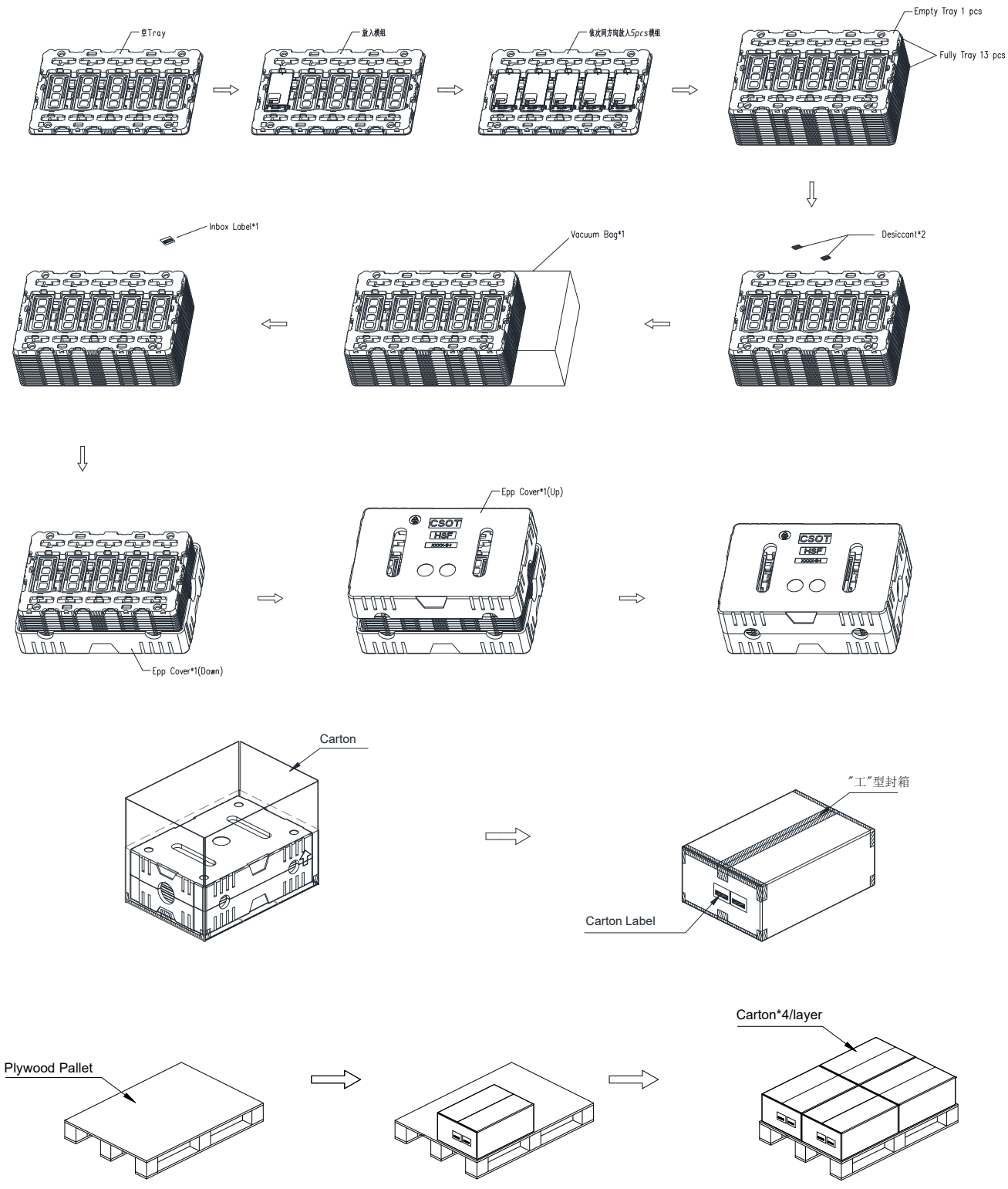
Part Name	Material	Thickness	Unit
CG		--	um
OCA		--	um
POL	SRWA62J-HC/L2/RWP/PC/7	106	um
Panel	/	40	um
BP	LS5625FA-S	88	um
Embo		--	um
Foam			
PI		--	um
Copper		--	um

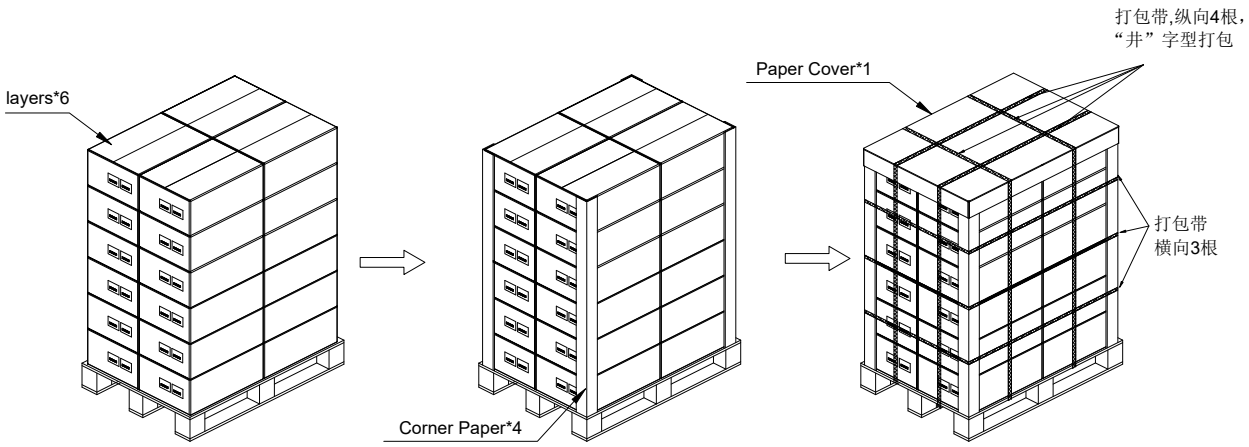
6 Package Drawing

6.1 Packing Specifications

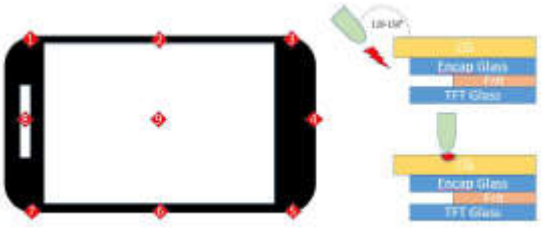
Item	Specification	Remark
Carton(Box) Packing	--	
Carton(Box) Packing Size	--	
Carton(Box) Packing Weight	--	For Reference
Pallet Packing	--	
Pallet Packing Size	--	
Pallet Packing Weight	--	For Reference

6.2 Packing Method




打包带,纵向4根，
“井”字型打包
layers*6
Paper Cover*1
打包带
横向3根
Corner Paper*4

7 RA Requirements

<table>
<tr><th>No.</th><th>Test Item</th><th>Test Condition</th></tr>
<tr><td>1</td><td>High Temperature High Humidity Operation</td><td>60℃, 90%RH ,240h</td></tr>
<tr><td>2</td><td>High Temperature Operation</td><td>70℃,240H</td></tr>
<tr><td>3</td><td>Low Temperature Operation</td><td>-20℃,240H</td></tr>
<tr><td>4</td><td>High Temperature Storage</td><td>80℃,240H</td></tr>
<tr><td>5</td><td>Low Temperature Storage</td><td>-40℃,240H</td></tr>
<tr><td>6</td><td>Thermal Shock</td><td>(-40℃/60min<->85℃/60min)，32cycles</td></tr>
<tr><td>7</td><td>ESD Test</td><td>ESD test by power off: TOLED Connector pin test, see table as follows.
ESD test by power on(Discharge model)
Ground: Contact & Air，150pF+330Ω;
Floating GND: Contact & Air，150pF+330Ω;
The location reference the table and Picture as below:
1. Point number: 1-3,5-7 (Contact); 1-9 (Air)
2. Times for each point: 10 times and between each test, 1s interval
3. Between each test should use electrostatic brush in the GND area of the TOLED, and export the charge to ensure that no charge added.
Test sample quantity=10pcs, and all 10 are required to pass the test.
<table>
<tr><th>Sample</th><th>Status</th><th>Test Mode</th><th>Spec. Level</th><th>Times</th><th>Judgement</th></tr>
<tr><td rowspan="6">TOLED</td><td rowspan="2">Power Off</td><td rowspan="2">Contact</td><td>±1KV</td><td rowspan="6">10</td><td>Power On Okay</td></tr>
<tr><td>±2KV</td><td>Power On Okay</td></tr>
<tr><td rowspan="4">Power On</td><td rowspan="2">Contact</td><td>±4KV</td><td>B</td></tr>
<tr><td>±6KV</td><td>B</td></tr>
<tr><td rowspan="3">Air</td><td>±4KV</td><td>B</td></tr>
<tr><td>±6KV</td><td>B</td></tr>
<tr><td>±8KV</td><td>B</td></tr>
</table>


Criteria A: after power-on test, TOLED should keep normal operation (no display or function abnormal).
Criteria B: after power - on test ,TOLED appear abnormal display 、TP failure or function failure ,but could recover to normal in 1s.
Criteria C: after power - on test , TOLED appear abnormal display 、TP failure or function failure, and could not automatically recover to normal, need rest or restart.</td></tr>
<tr><td>8</td><td>On off test</td><td>25℃±2℃，On 3s，Off 3s，1500 times</td></tr>
</table>

<table>
<tr><td>9</td><td>HT touch test</td><td>6h&50℃, Storage, Touch function test should be OK</td></tr>
<tr><td>10</td><td>LT touch test</td><td>6h&-20℃, Storage, Touch function test should be OK</td></tr>
<tr><td>11</td><td>Package Test</td><td>50℃ 80%RH, Storage 2hr
Vibration Test: Frequency 5Hz, Amplitude 20mm.
Direction: X,Z; X and Z each 60min.
Package Drop Test (Direction) : 1Angle, 3Edge, 6Face;
Drop height refer to the table as below.
<table><tr><th>包装总重量</th><th>跌落高度（CM)</th></tr><tr><td>10KG以下</td><td>80</td></tr><tr><td>10KG~20KG</td><td>60</td></tr><tr><td>20KG~30KG</td><td>50</td></tr><tr><td>30KG~40KG</td><td>40</td></tr></table></td></tr>
</table>

8 General Precautions

Please pay attention to the following items when you use the OLED Modules(Panel):

8.1 Do not twist or bend the module(panel) and prevent the unsuitable external force for display during assembly.

8.2 Adopt measures for good heat radiation. Be sure to use the module(panel) with in the specified temperature.

8.3 Avoid dust or oil mist during assembly.

8.4 Follow the correct power sequence while operating. Do not apply the invalid signal, otherwise, it will cause improper shut down and damage the module(panel).

8.5 Less EMI: it will be more safety and less noise.

8.6 Please operate module(panel) in suitable temperature. The response time & brightness will drift by different temperature.

8.7 Avoid to display the fixed pattern (exclude the white pattern) in a long period, otherwise, it will cause image sticking.

8.8 Please be sure to turn-off the power when connecting or disconnecting the circuit.

8.9 Polarizer scratches easily, please handle it carefully.

8.10 Display surface never likes dirt or stains.

8.11 A dew drop may lead to destruction. Please wipe off any moisture before using module(panel).

8.12 Sudden temperature changes cause condensation, and it will cause polarizer damaged.

8.13 High temperature and humidity may degrade performance. Please do not expose the module(panel) to the direct sunlight and so on.

8.14 Acetic acid or chlorine compounds are not friends with AMOLED display module(panel).

8.15 Static electricity will damage the module(panel), please do not touch the module(panel) without any grounded device.

8.16 Please avoid any static electricity damage (ESD) during producing and operating.

8.17 Do not disassemble and reassemble the module(panel) by self.

8.18 Be careful do not touch the rear side directly.

8.19 No strong vibration or shock. It will cause module(panel) broken.

8.20 Store the module in a dark room where must keep at 25±10℃ and 65%RH or less.

8.21 Do not store the module in surroundings containing organic solvent or corrosive gas.

8.22 Be careful of injury from a broken display module(panel).

8.23 Please avoid the pressure adding to the surface (front or rear side) of modules(panel), because it will cause the display.